Low Power, Rail-to-Rail Output Precision JFET Amplifier

AD8641/AD8642

FEATURES

Low supply current: 250 µA max
Very low input bias current: 1 pA max
Low offset voltage: 750 µV max
Single-supply operation: 5 V to 26 V
Dual-supply operation: ±2.5 V to ±13 V
Rail-to-rail output
Unity gain stable
No phase reversal
SC70 package

APPLICATIONS

Line-/battery-powered instruments
Photodiode amplifiers
Precision current sensing
Medical instrumentation
Industrial controls
Precision filters
Portable audio
ATE

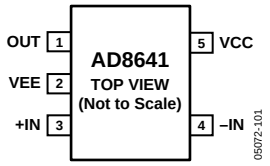

Figure 1. 5-Lead SC70 (KS-5)

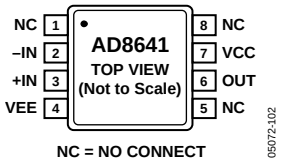

Figure 2. 8-Lead SOIC (R-8)

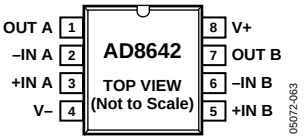

Figure 3. 8-Lead SOIC (R-8)

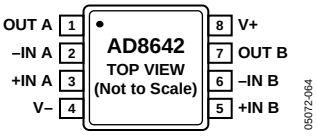

Figure 4. 8-Lead MSOP (RM-8)

GENERAL DESCRIPTION

The AD8641/AD8642 are low power, precision JFET input amplifiers featuring extremely low input bias current and rail-to-rail output. The ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables designers to buffer CMOS DACs, ASICs, and other wide output swing devices in single-supply systems. The outputs remain stable with capacitive loads of more than 500 pF.

The AD8641/AD8642 are suitable for applications utilizing multichannel boards that require low power to manage heat. Other applications include photodiodes, ATE reference level drivers, battery management, and industrial controls.

The AD8641/AD8642 are fully specified over the extended industrial temperature range of –40°C to +125°C. The AD8641 is available in 5-lead SC70 and 8-lead SOIC lead-free packages. The AD8642 is available in 8-lead MSOP and 8-lead SOIC lead-free packages.

Rev. A
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REVISION HISTORY

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10/04—Initial Version: Revision 0

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			50	750	µV
		–40°C < T_A < +85°C			1.5	mV
		+85°C < T_A < +125°C, V_{CM} = 1.5 V			1.6	mV
Input Bias Current	I_B			0.25	1	pA
		–40°C < T_A < +125°C			180	pA
Input Offset Current	I_{OS}				0.5	pA
		–40°C < T_A < +125°C			60	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	74	93		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 to 4.5 V	80	140		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		4.95			V
		I_L = 1 mA, –40°C to +125°C	4.94			V
Output Voltage Low	V_{OL}				0.05	V
		I_L = 1 mA, –40°C to +125°C		0.01	0.05	V
Output Current	I_{OUT}			±6		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 26 V	90	107		dB
Supply Current/Amplifier	I_{SY}			195	250	µA
		–40°C < T_A < +125°C			270	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			2		V/µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	$Ø_O$			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.0		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		28.5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.5		fA/√Hz

@ V_S= ±13 V, V_{CM} = 0 V, T_A =25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			70	750	µV
		−40° < T_A < +125°C			1.5	mV
Input Bias Current	I_B			0.25	1	pA
		−40°C < T_A < +125°C			260	pA
Input Offset Current	I_{OS}				0.5	pA
		−40°C < T_A < +125°C			65	pA
Input Voltage Range			−13		+10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -13 V to +10 V	90	107		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −11 V to +11 V	215	290		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		+12.95			V
		I_L = 1 mA, −40°C to +125°C	+12.94			V
Output Voltage Low	V_{OL}				−12.95	V
		I_L = 1 mA, −40°C to +125°C			−12.94	V
Output Current	I_{OUT}			±12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±13 V	90	107		dB
Supply Current/Amplifier	I_{SY}			200	290	µA
		−40°C < T_A < +125°C			330	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			3		V/µs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	Ø**o**			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.2		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		27.5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.5		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.[1]

Parameter	Rating
Supply Voltage	27.3 V
Input Voltage	VS– to VS+
Differential Input Voltage	±Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
KS-5, R-8, RM-8 Packages	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	
KS-5, R-8, RM-8 Packages	–65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4.

Package Type	θ_{JA}[2]	θ_{JC}	Unit
5-Lead SC70 (KS-5)	331.4	223.9	°C/W
8-Lead SOIC (R-8)	157	56	°C/W
8-Lead MSOP (RM-8)	206	44	°C/W

[1] Absolute maximum ratings apply at 25°C, unless otherwise noted.
[2] θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for devices soldered on circuit boards for surface-mounted packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

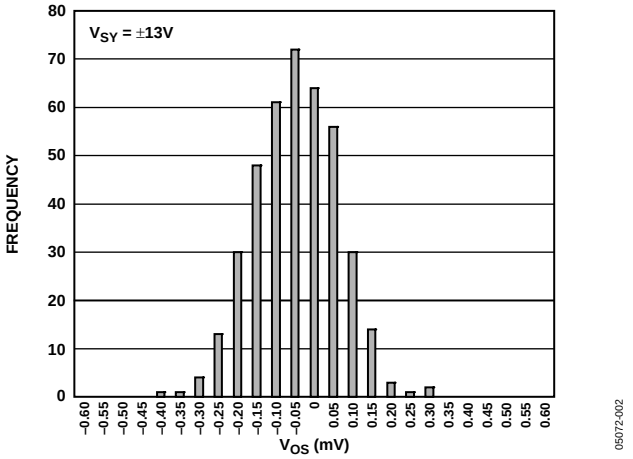

Figure 5. Input Offset Voltage

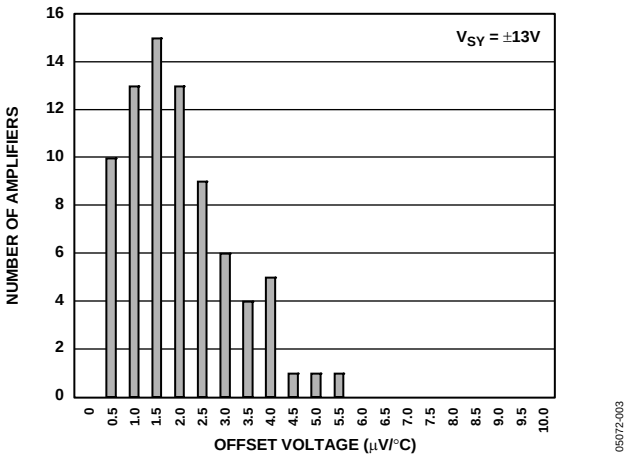

Figure 6. Offset Voltage Drift

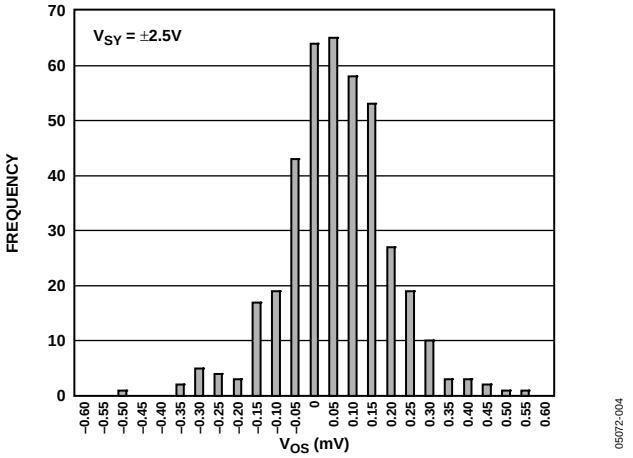

Figure 7. Input Offset Voltage

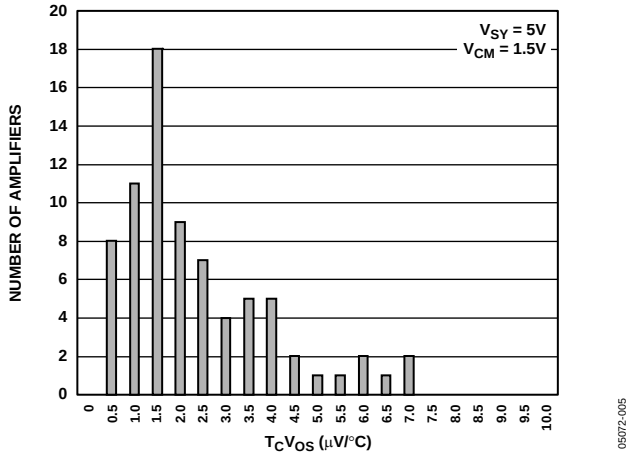

Figure 8. Offset Voltage Drift

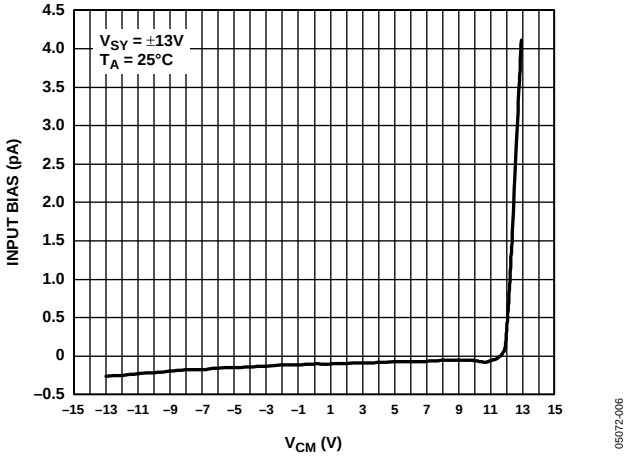

Figure 9. Input Bias Current vs. V_{CM}

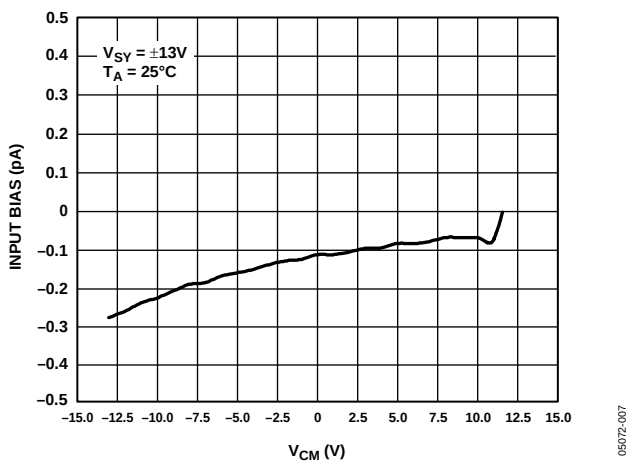

Figure 10. Input Bias Current vs. V_{CM}

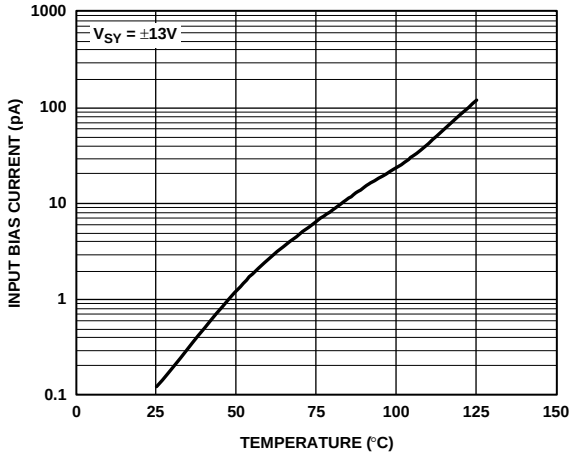

Figure 11. Input Bias Current vs. Temperature

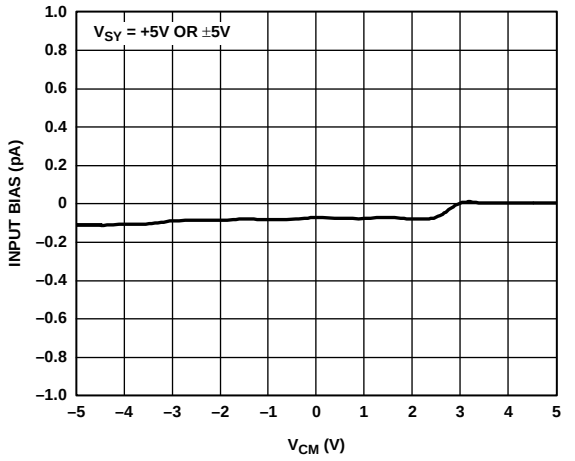

Figure 12. Input Bias Current vs. V_{CM}

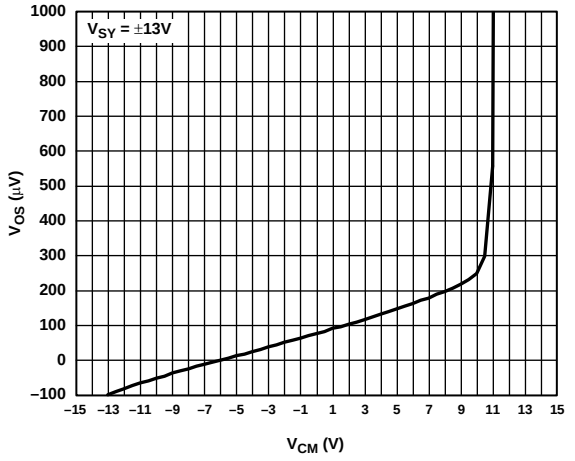

Figure 13. Input Offset Voltage vs. V_{CM}

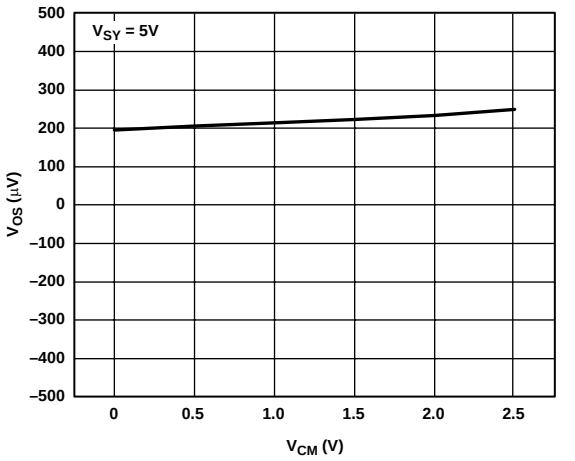

Figure 14. Input Offset Voltage vs. V_{CM}

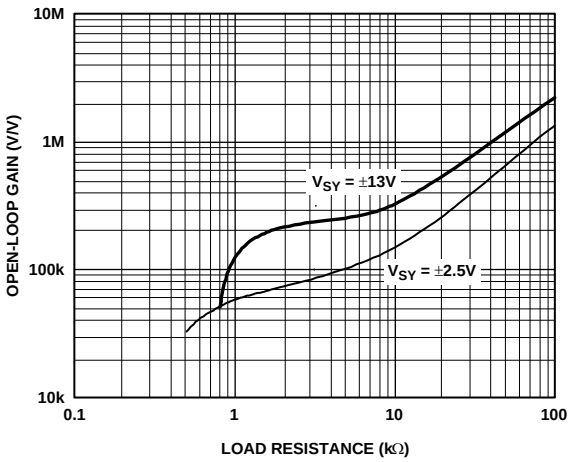

Figure 15. Open-Loop Gain vs. Load Resistance

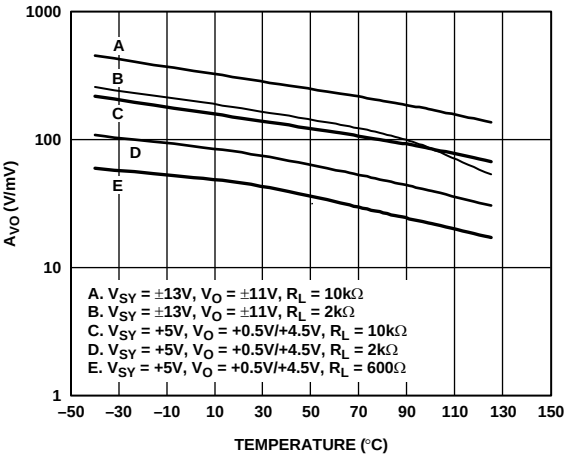

Figure 16. Open-Loop Gain vs. Temperature

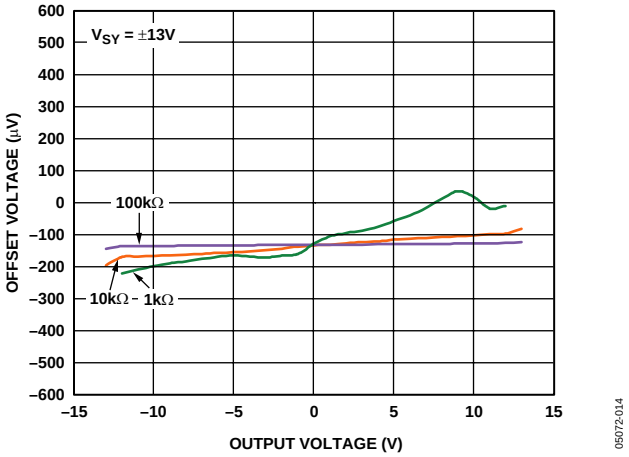

Figure 17. Input Error Voltage vs. Output Voltage for Resistive Loads

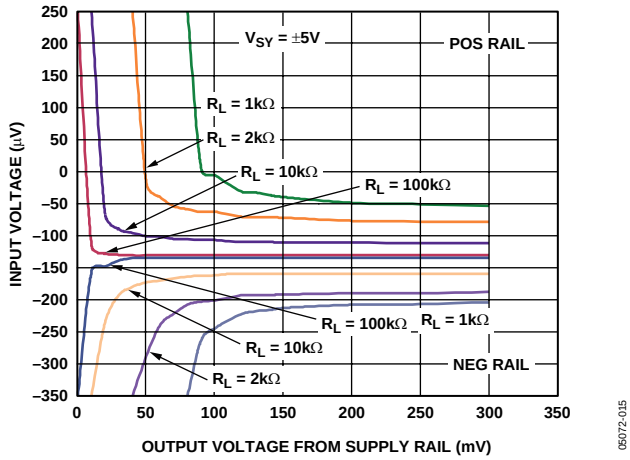

Figure 18. Input Error Voltage vs. Output Voltage Within 300 mV of Supply Rails

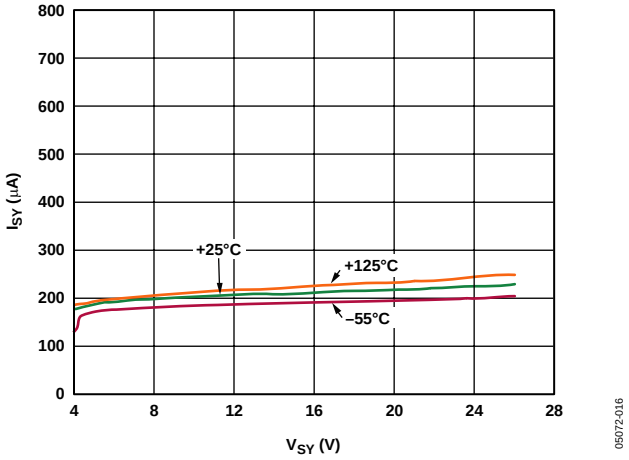

Figure 19. Quiescent Current vs. Supply Voltage at Different Temperatures

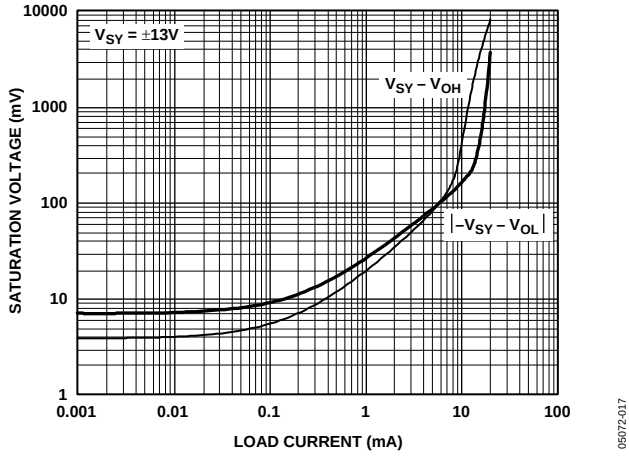

Figure 20. Output Saturation Voltage vs. Load Current

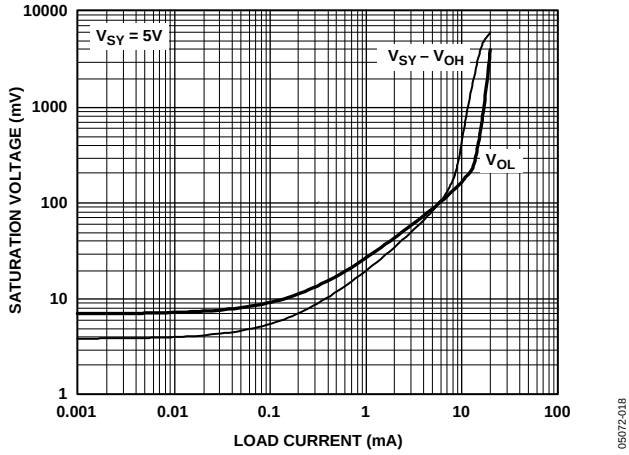

Figure 21. Output Saturation Voltage vs. Load Current

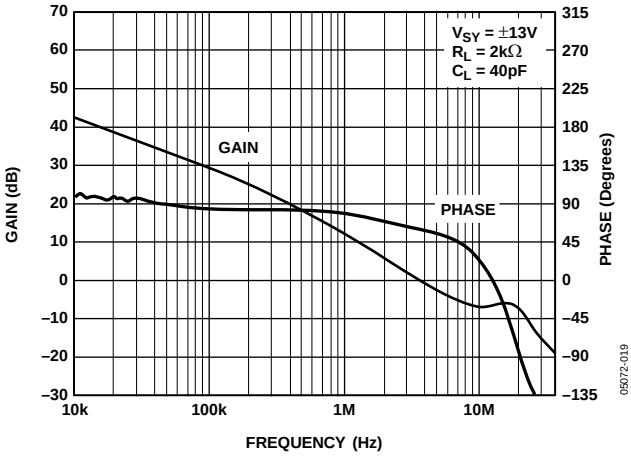

Figure 22. Open-Loop Gain and Phase Margin vs. Frequency

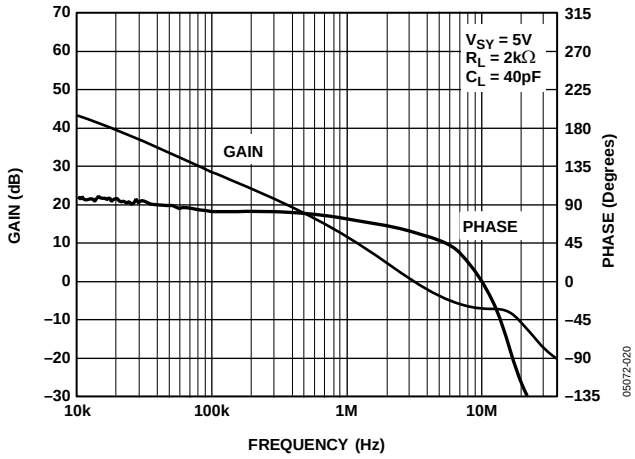

Figure 23. Open-Loop Gain and Phase Margin vs. Frequency

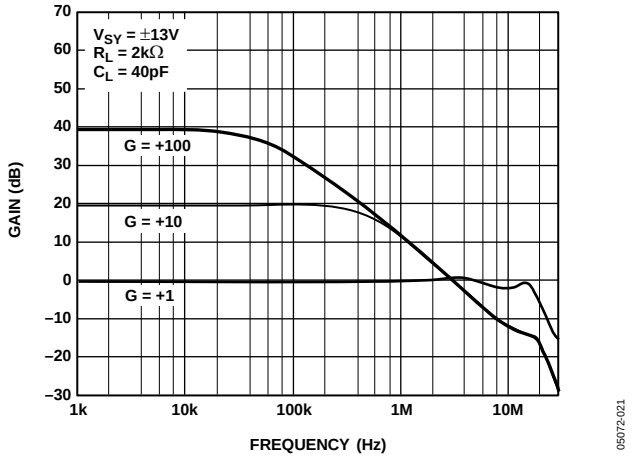

Figure 24. Closed-Loop Gain vs. Frequency

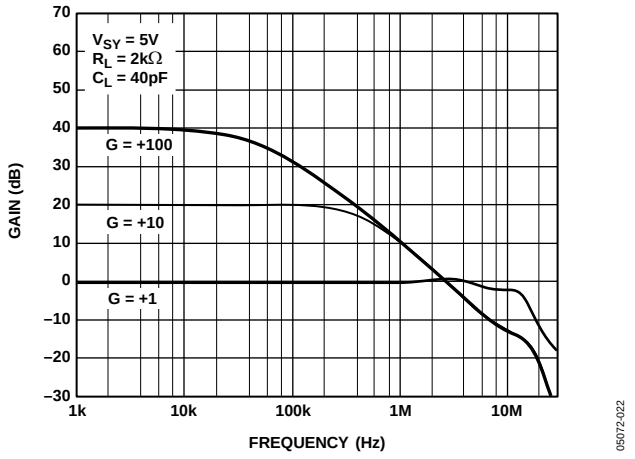

Figure 25. Closed-Loop Gain vs. Frequency

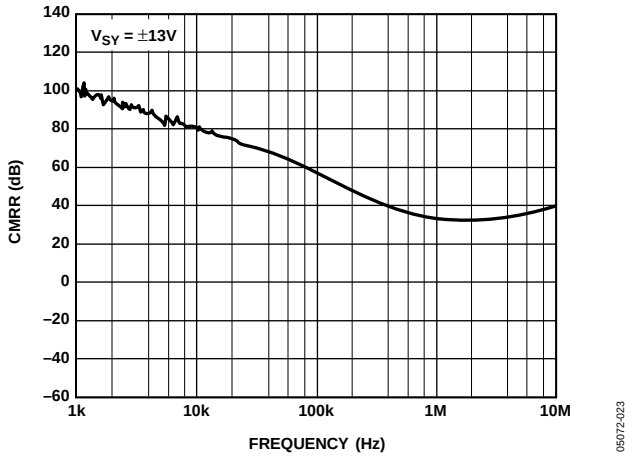

Figure 26. CMRR vs. Frequency

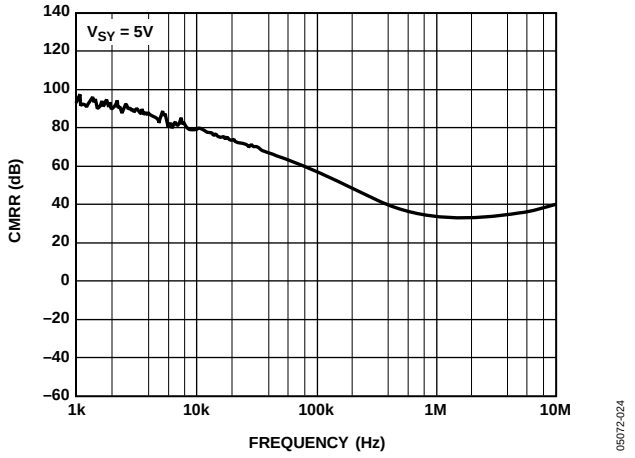

Figure 27. CMRR vs. Frequency

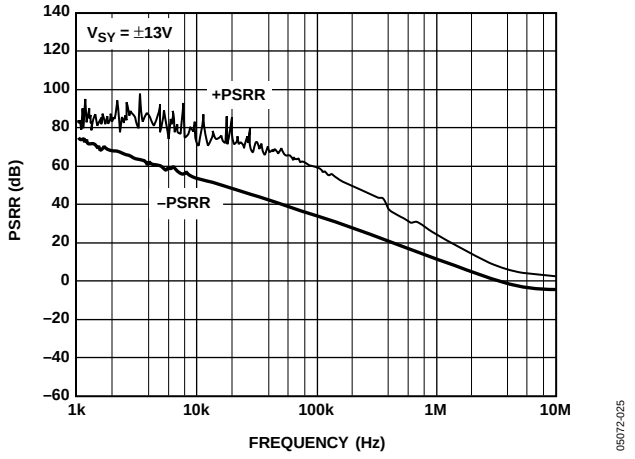

Figure 28. PSRR vs. Frequency

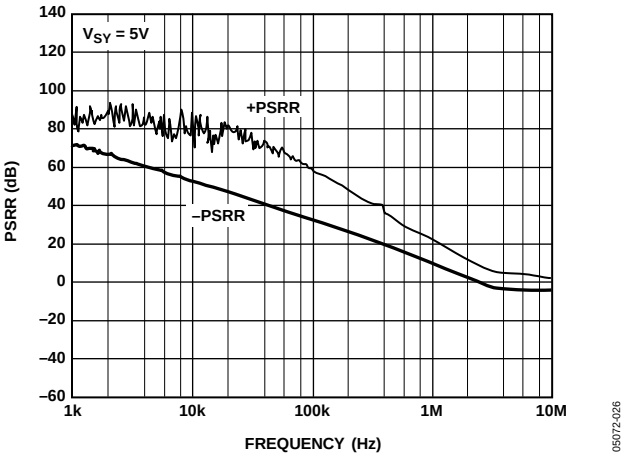

Figure 29. PSRR vs. Frequency

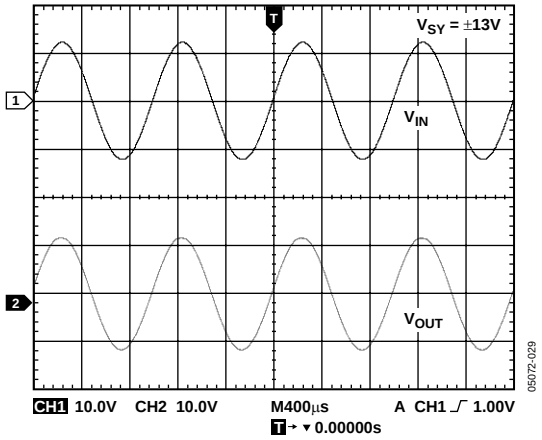

Figure 32. No Phase Reversal

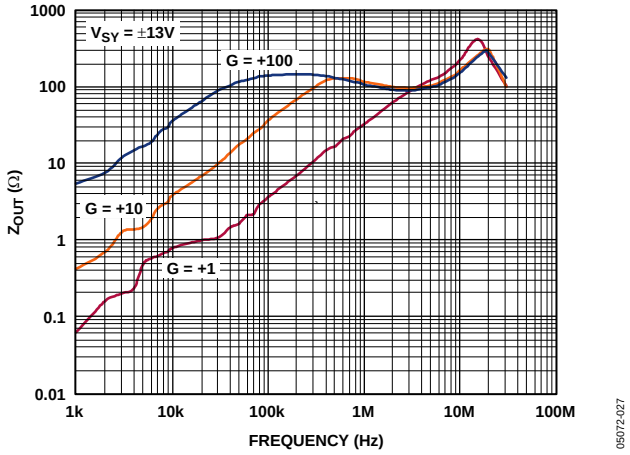

Figure 30. Output Impedance vs. Frequency

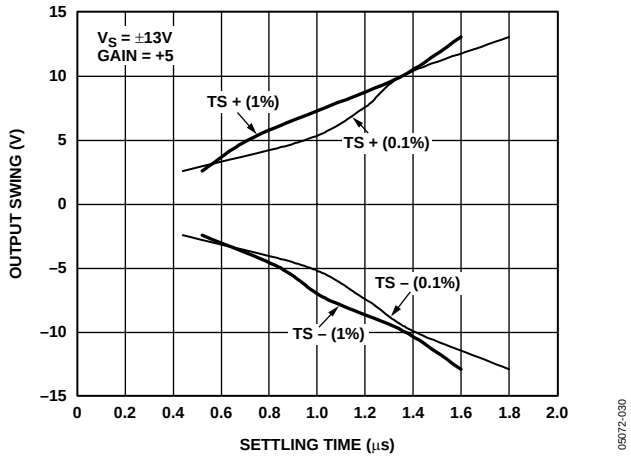

Figure 33. Output Swing and Error vs. Settling Time

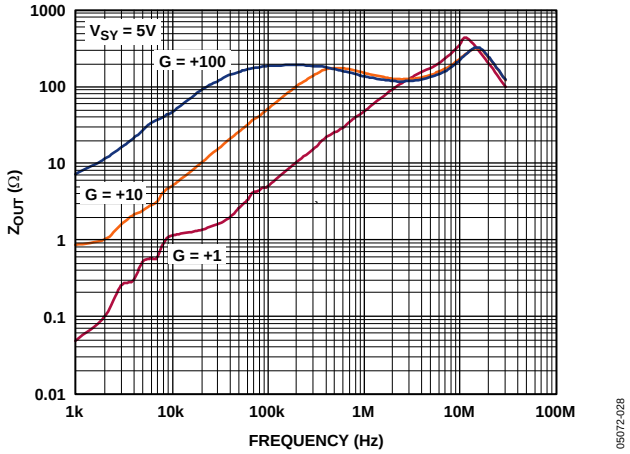

Figure 31. Output Impedance vs. Frequency

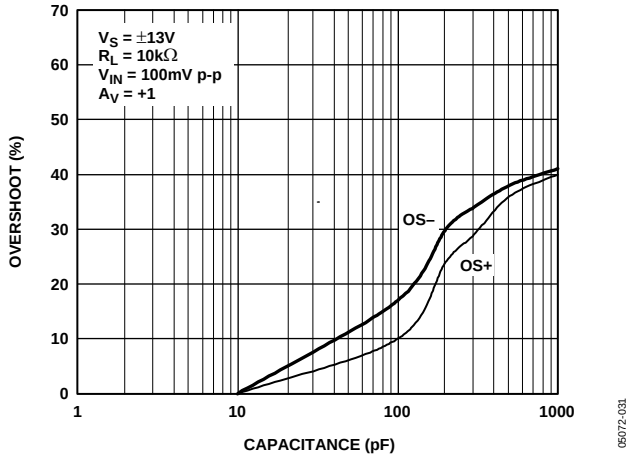

Figure 34. Small Signal Overshoot vs. Load Capacitance

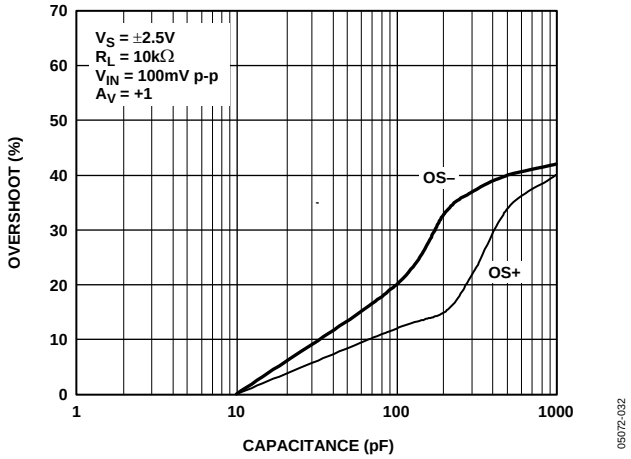

Figure 35. Small Signal Overshoot vs. Load Capacitance

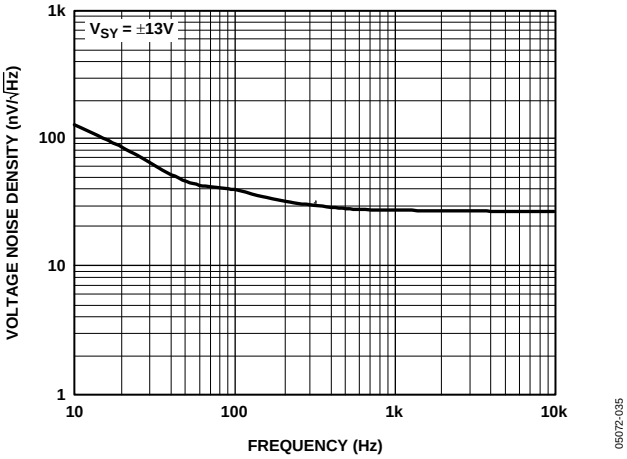

Figure 38. Voltage Noise Density

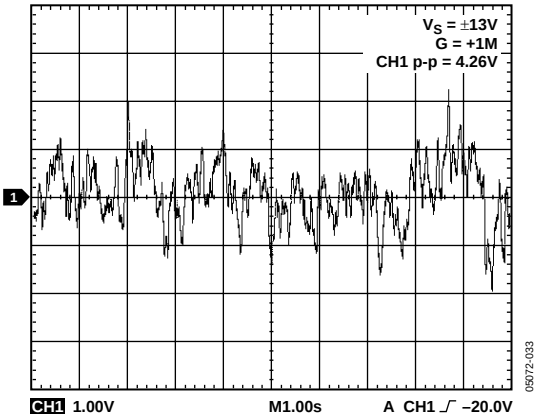

Figure 36. 0.1 Hz to 10 Hz Noise

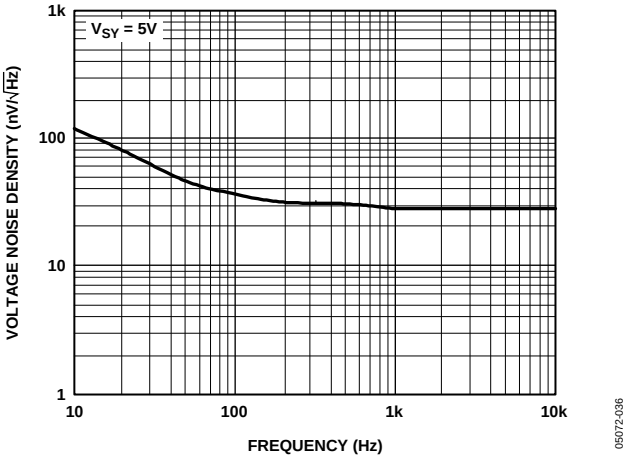

Figure 39. Voltage Noise Density

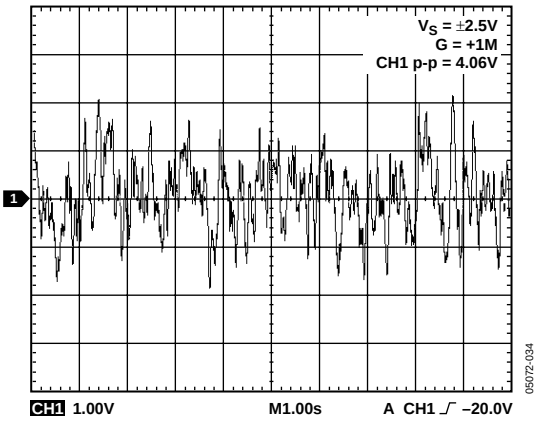

Figure 37. 0.1 Hz to 10 Hz Noise

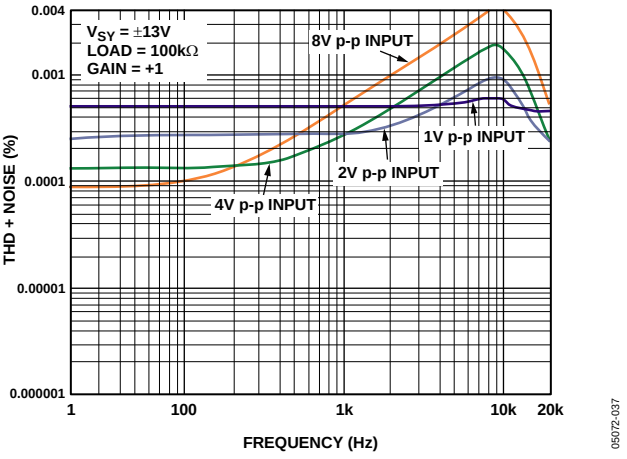

Figure 40. Total Harmonic Distortion + Noise vs. Frequency

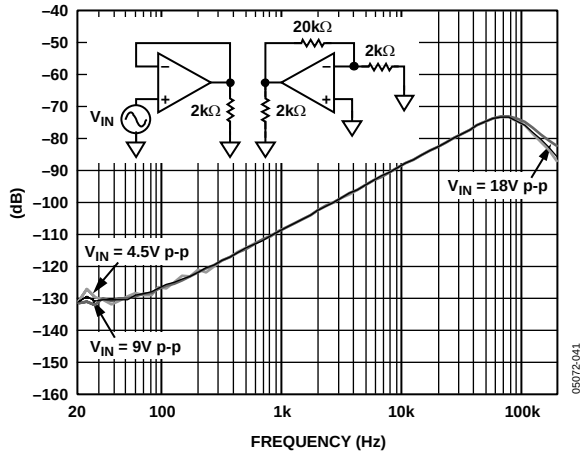

Figure 41. Channel Separation

OUTLINE DIMENSIONS

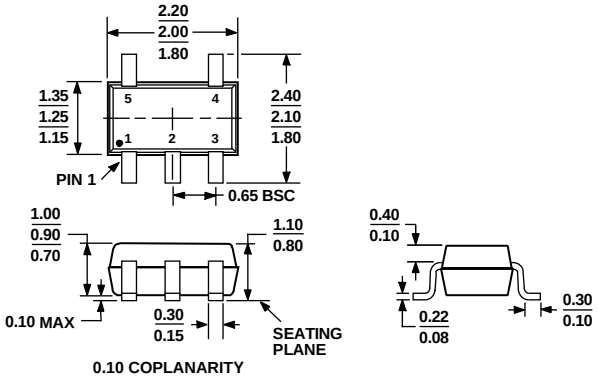

Figure 42. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

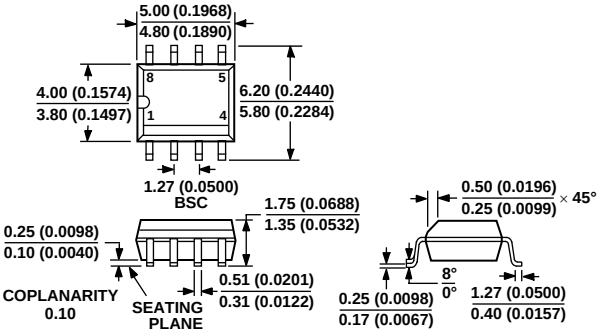

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
(R-8)
Dimensions shown in millimeters and (inches)

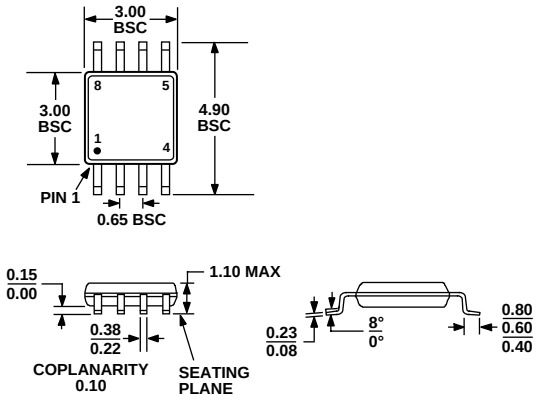

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8641AKSZ-R2[1]	–40°C to +125°C	5-Lead SC70	KS-5	A07
AD8641AKSZ-REEL7[1]	–40°C to +125°C	5-Lead SC70	KS-5	A07
AD8641AKSZ-REEL[1]	–40°C to +125°C	5-Lead SC70	KS-5	A07
AD8641ARZ[1]	–40°C to +125°C	8-lead SOIC_N	R-8	
AD8641ARZ-REEL7[1]	–40°C to +125°C	8-lead SOIC_N	R-8	
AD8641ARZ-REEL[1]	–40°C to +125°C	8-lead SOIC_N	R-8	
AD8642ARMZ-R2[1]	–40°C to +125°C	8-lead MSOP	RM-8	A0A
AD8642ARMZ-REEL[1]	–40°C to +125°C	8-lead MSOP	RM-8	A0A
AD8642ARZ[1]	–40°C to +125°C	8-lead SOIC	R-8	
AD8642ARZ-REEL7[1]	–40°C to +125°C	8-lead SOIC	R-8	
AD8642ARZ-REEL[1]	–40°C to +125°C	8-lead SOIC	R-8	

[1] Z = Pb-free part.

NOTES

NOTES

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